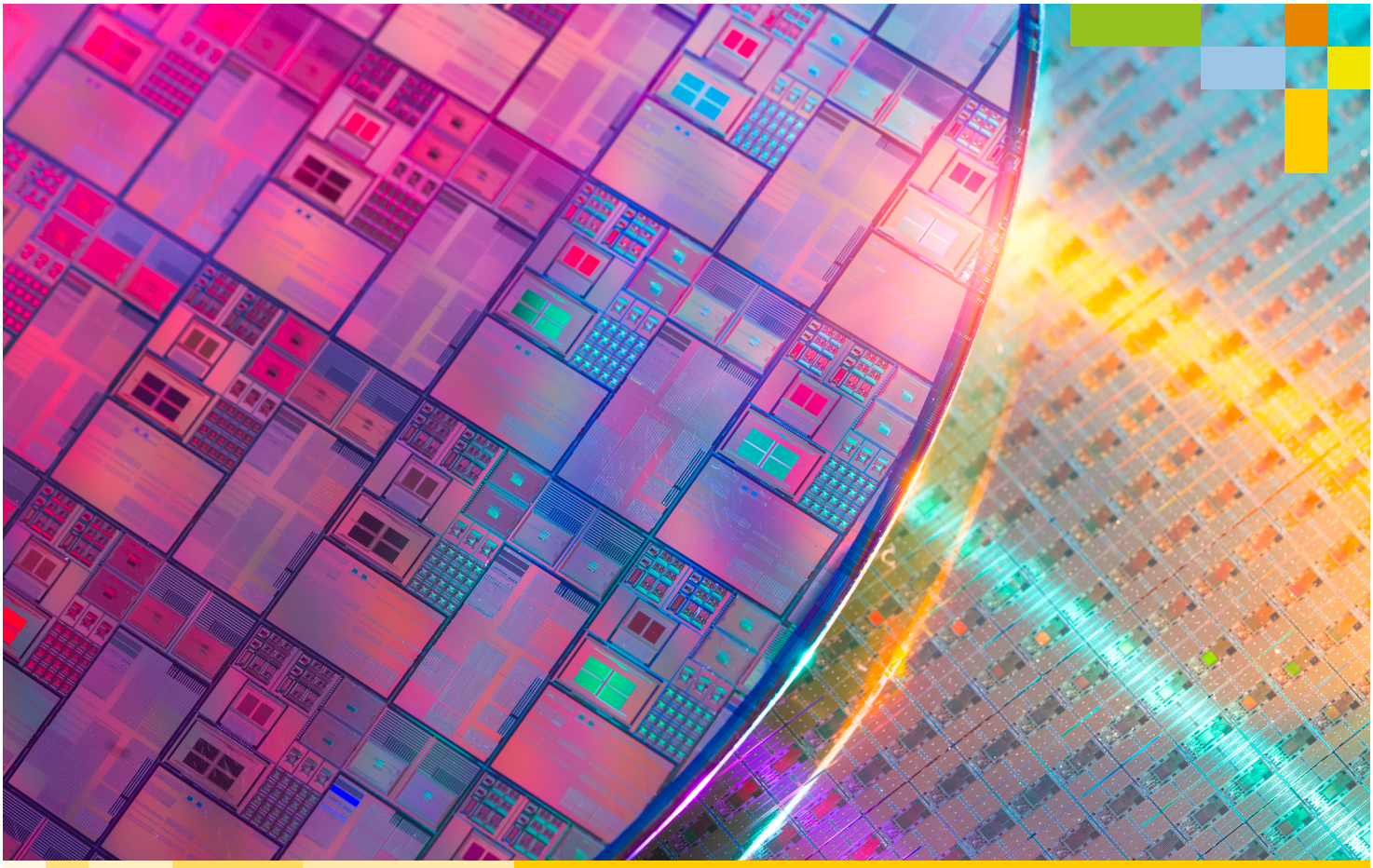

acatech IMPULSE

RISC-V

An Open Standard for Chip Development

Christoph Kutter (Ed.)

acatech
NATIONAL ACADEMY OF SCIENCE AND ENGINEERING

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The acatech IMPULSE series

This series comprises contributions to debates and thought-provoking papers on strategic engineering and technology policy issues. IMPULSE publications discuss policy options and are aimed at decision-makers in government, science and industry, as well as interested members of the general public. Responsibility for the contents of IMPULSE publications lies with their authors.

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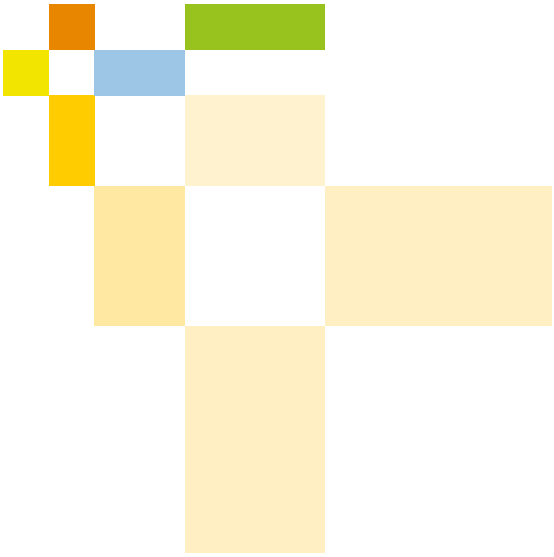

Executive summary

The chip crisis in early 2020 clearly demonstrated the degree to which Germany and indeed all of Europe are dependent on the supply of microelectronic components. Despite experts repeatedly emphasising the importance of this industry to Europe's capacity for innovation, shortages occurred which threatened major industrial sectors. Boosting Europe's semiconductor ecosystem is key to reducing this dependency and strengthening innovative capacity in significant applications such as automotive. In response to this need, the European Chips Act is being drawn up and the pace of establishing chip fabrication facilities in Europe is being stepped up.

In addition to semiconductor fabrication, another important factor in ensuring Europe's technological sovereignty is to strengthen innovative chip development capabilities by providing appropriate specialist personnel. In this context, theinstruction set architecture RISC-V holds great promise because, as an open standard, it eliminates many, sometimes problematic, constraints of proprietary instruction sets. This promotes innovation in microelectronics because RISC-V, as an open standard, can be freely used and flexibly adapted to the requirements of the particular application and domain, for example by individual extensions of the instruction set to increase efficiency. Moreover, being a licence-free standard, RISC-V can be used at low cost in universities, so enabling students and researchers to independently develop and implement innovative approaches to chip design. A licence-free standard also facilitates transfer to application by spin-offs and start-ups. In addition, using RISC-V reduces the impact of geopolitical pressure because import and export restrictions are not directly applicable to open standards. This boosts the innovator's technological sovereignty.

These opportunities mean that the RISC-V open standard is attracting considerable interest from academia and industry. This trend should be further encouraged by investing in a robust and widely available development infrastructure to promote resilience and technological sovereignty.

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Project duration

01/2023 –11/2023

1 Current global developments

Microprocessors are the foundation of our digitalised lives. While in the past these technologically comparatively complex products were primarily used in high-priced, complicated appliances, today they are also used for controlling simple applications such as lighting, thermostats or simple pushbutton switches.

Microprocessor technology and the associated semiconductor market have developed in recent decades from a primarily heterogeneous situation into a market with two major standards and indeed the simple processor market is dominated by just one standard.

A processor's instruction set determines the interface between the hardware and software, i. e. defines the machine instructions which are executed. While thirty years ago numerous microprocessor architectures and instruction sets were available for a wide range of applications and were in competition with one another (PowerPC, SPARC, Renesas, MIPS, Tensilica etc.), the field for complex architectures has largely consolidated into two proprietary solutions: Intel's x86 architecture and Arm Holdings plc's Arm© architecture[1]. x86 architecture is designed for powerful desktop PCs and servers while the compact Arm© architecture is ideally suitable for use in mobile devices due to its low energy consumption.

On the back of the meteoric growth in mobile telephony [2], Arm© architecture also became increasingly significant and has ultimately gained a dominant market position and expanded into further applications ranging from small controllers to high-performance processors for desktops[3] and servers[4].

Since the architecture is widely used and has a strong ecosystem consisting of know-how and available expertise, development tools (e. g. software tools) and suitable off-the-shelf components, ever more companies are using this standard and licensing it for further products instead of investing considerable effort and funds in developing and maintaining their own architectures. The resultant dependency is accepted, although geopolitical changes and their consequences for the market as well as possible changes in ownership could have a critical impact on the user company.

Such extensive dependency on a single supplier was accepted because until the late 2010s the semiconductor market was considered global and the risk of dependency was not given a high priority.

In more recent years, attitudes have been changed by geopolitical conflicts and global crises such as the Covid-19 pandemic, which have impacted global trade relations. It can now no longer be assumed that every microelectronics component or technology will be freely available on a free global market. An ability to develop microprocessors and microcontrollers and the availability of suitable manufacturing facilities are now understood to be fundamental to technological sovereignty.[5] Access to microelectronic components and manufacturing facilities is used as political leverage in the context of restraints on trade.[6, 7]

A further aspect to be borne in mind is the slowdown in Moore's law (see information box) which means that new technological approaches and architectures are increasingly required to achieve higher performance, for instance by specific accelerators for artificial intelligence applications. Proprietary solutions only permit the instruction set customisations desired for this purpose with a specific architecture licence.

Moore's law

Moore's law is a rule of thumb based on empirical observation that states that the number of transistors per unit area doubles every 18 to 24 months. However, development is now coming up against physical limits. Whereas in the past it has been possible to boost performance primarily by miniaturisation, today new materials, new component architectures and 3D integration are required.

1 | To simplify readability, this publication, like https://www.arm.com/architecture, draws no distinction between instruction set architecture and microarchitecture.
2 | https://de.statista.com/statistik/daten/studie/256337/umfrage/prognose-zum-weltweiten-absatz-von-tablets-pcs-und-smartphones/
3 | https://support.apple.com/de-de/HT211814
4 | https://aws.amazon.com/de/ec2/graviton/
5 | See acatech 2021.
6 | https://www.tagesschau.de/multimedia/sendung/tagesschau_20_uhr/video-541521.html
7 | https://www.tagesschau.de/ausland/amerika/usa-china-huawei-101.html

Being an open standard, the new RISC-V[8] instruction set can address many of these challenges in new ways and so provides an alternative to proprietary instruction sets. As an open and licence-free standard, developers can extend it as desired, so enabling individual modifications for innovative processors. In addition, a RISC-V based product is less bound by (commercial) terms and conditions than would be the case if proprietary instruction sets were used. Counterbalancing these advantages, RISC-V currently sometimes requires considerably greater development and support input, since the necessary tools are often not yet available. It is therefore to be expected that in microelectronics, similar to the software industry with Linux and Windows, licence-free and proprietary solutions will coexist and may be more suitable depending on the use case. RISC-V is currently the subject of intensive investigation and discussion, for example in the ASPECT study funded by the Federal Ministry of Education and Research (BMBF) and published in 2023.[9] Internationally, RISC-V is currently strongly in the ascendant, as is clear from the rapidly increasing membership of RISC-V International, the non-profit which maintains and further develops the standard. RISC-V based processors are already in use in numerous products[10] and demanding applications such as data centres or machine learning[11] Even large companies are now publicly communicating their RISC-V activities.[12]

More widespread adoption of RISC-V could in particular strengthen Germany as a place to innovate and do business. While positions in proprietary instruction sets have been entrenched for decades, in the dynamic RISC-V environment significant opportunities are open to new players to build a strong position in this innovative ecosystem.

The aims of this IMPULSE are to describe RISC-V, to indicate to political and business decision-makers the opportunities and threats of the open standard, and to offer a clear illustration of some example applications. Finally, recommendations for academia, business and policy makers will be set out.

Special situation: RISC-V and China

China is increasingly investing in the development and use of RISC-V to reduce dependency on foreign technology suppliers and strengthen national sovereignty in the semiconductor field. Chinese companies and research institutions are working hard to develop RISC-V-based processors and, as a result, China is becoming a major player in the RISC-V community. In China, RISC-V is primarily being driven forward by the government and government-related organisations to ensure technological sovereignty in the face of US sanctions. The "China RISC-V Alliance" was thus founded in 2018 with the aim of developing a comprehensive open-source chip design ecosystem by 2030. In 2019, the Chinese Academy of Science established a national initiative to advance RISC-V in China. However, this has raised geopolitical tensions, with the US and other countries expressing concerns about potential technology transfers and security risks. For example, a competitive, RISC-V based processor is set to be developed collaboratively with Alibaba, Tencent and ZTE. Most recently, a patent pooling organisation was, for example, also announced at RISC-V Summit China.[13]

8 | RISC stands for Reduced Instruction Set Computer (see information box) while V relates to the fifth generation of RISC architectures which have been under development at the University of California, Berkeley since 1981.
9 | https://elektronikforschung.de/service/publikationen/risc-v-oekosystem-status-und-potenzial
10 | https://riscv.org/announcements/2022/12/risc-v-sees-significant-growth-and-technical-progress-in-2022-with-billions-of-risc-v-cores-in-market/
11 | See Kalapothas et al. 2023.
12 | https://www.bosch-presse.de/pressportal/de/en/leading-semiconductor-industry-players-join-forces-to-accelerate-risc-v-257024.html
13 | https://www.theregister.com/2023/08/31/china_risc_v_patent_alliance/

2 RISC-V – What is it?

RISC-V is an open standard for an instruction set architecture which is an essential part of a computer system and forms the interface between software and hardware by specifying which machine instructions a processor can handle and how these are to be mapped in hardware. The following description of the individual layers of the abstract computer architecture clarifies the role of the instruction set (see figure 1).

Algorithm and application

The application and associated algorithm are the highest layer of a computer system. The algorithm defines system behaviour, for example the response to an input or modified sensor value.

Program code

The program code is the implementation of the algorithm in "high-level" language such as C. However, it is not directly readable by the processor but must instead be converted by a compiler into a form executable by the processor.

Assembler/binary code

This layer describes the processor-readable form of the program code which describes the algorithm. While this form can still be viewed and edited by humans, it is highly detailed and difficult for humans to interpret. This layer is part of the instruction set architecture, defining which assembler/machine instructions the computer system's processor can handle in software and how these instructions are coded as a binary sequence of zeros and ones.

Hardware architecture

At the hardware level, the coding guidelines for the instruction set determine how the state of the machine is being changed by specific instructions. Implementation as a combination of memory elements and logic devices in the "microarchitecture" may vary greatly for one and the same instruction set, depending on the given constraints such as target frequency, software performance or energy consumption. This microarchitecture is the central technical and economic differentiating factor between different manufacturers of processors using the same instruction set.

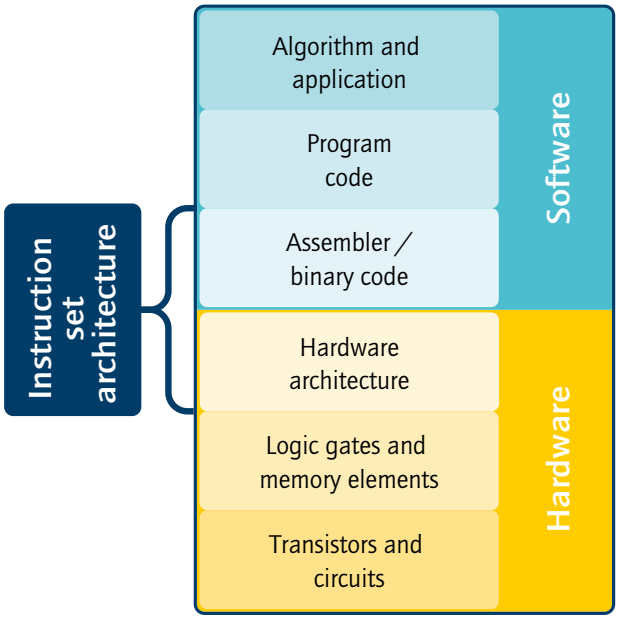

Figure 1: Layers of a computer system (source: own presentation)

Logic gates and memory elements

These are the basis on which the microarchitecture is constructed and implement it in the form of arithmetic operations such as addition and subtraction or as control instructions.

Transistors and circuits

These are the foundation of an electronic computer system and are used to build the logic gates, arithmetic units and memory elements.

RISC and CISC: two different design classes for microprocessors

RISC: Reduced Instruction Set Computer
denotes an architecture with a lean instruction set which can be implemented very efficiently. It was introduced in the mid-1980s and has since been considered a major breakthrough in achieving significant performance improvements.

CISC: Complex Instruction Set Computer
denotes an architecture with an extensive instruction set capable of executing complex instructions in a single computing step. Until the 1990s, computer systems were implemented using this approach because it offered high efficiency under the constraints which applied at that time. It has effectively been replaced by RISC in powerful systems.

Although the instruction set remains invisible to end users as the interface between hardware and software, it is of central importance because the software is tailored to it. This is why, when the instruction set is changed, the software often also has to be adapted, which is a time-consuming and costly undertaking.

Currently, two instruction sets dominate the entire computer industry: x86 from Intel and AMD as comparatively extensive instruction sets (CISC) for high-performance computing (HPC) and data centres, desktop PCs, notebooks and servers and the Arm© architecture from Arm Holdings plc as a compact instruction set (RISC) for mobile terminals and relatively small microprocessors in numerous computer-controlled products and increasingly also in notebooks, desktop PCs and data centres. Neither of these instruction sets is an open standard but instead require licensing agreements between the companies concerned. The challenges facing the semiconductor industry in terms of supply chains, adaptability to innovative chip platforms, and the geopolitical situation highlight the problems of proprietary licensing models.

One alternative to proprietary instruction sets which require licences are open standards, as are available for many other software and hardware components of a modern computer system. RISC-V, under development at the University of California, Berkeley since 2010 and published as an open standard in 2014, is one such open instruction set. Maintenance of the standard is the responsibility of the non-profit RISC-V International (formerly RISC-V Foundation), which has relocated its headquarters to Switzerland to ensure neutrality.[14] Since then, the standard has experienced active participation and adaptation and, after many years of definition, is on the cusp of expanding into various domains such as computing and data centres, the automotive sector or industrial processors.

The core of the instruction set is minimalistic. Extensions make it possible to implement different types of processor design and so optimise for the particular needs of individual use cases. These extensions are developed in a joint community effort and standardised by RISC-V International. There are no licensing costs other than the cost of membership required to use the RISC-V trademark. At the same time, it is possible to make individual modifications and extensions to the RISC-V instruction set which need not necessarily be coordinated, communicated or shared with the community.

The combination of openness, modularity and extensibility makes RISC-V of great interest, especially for European stakeholders active in highly specialised domains. The resulting new opportunities permit technical diversification, so strengthening technological sovereignty and encouraging the emergence of innovative or disruptive as well as powerful and resource-optimised platforms for various systems. Figure 2 shows this combination of potential benefits of RISC-V, which arise from the competition fostered by an open standard.

The following sections present the opportunities which RISC-V offers to both academic and industrial research (see section 2.1), the geopolitical advantages which arise from the possibilities of strengthening technological sovereignty (see section 2.2), and the technical design latitude available with RISC-V (see section 2.3). We will also discuss the challenges of using RISC-V (see section 2.4).

14 | https://www.eetimes.eu/risc-v-to-move-hq-to-switzerland-amid-trade-war-concerns/

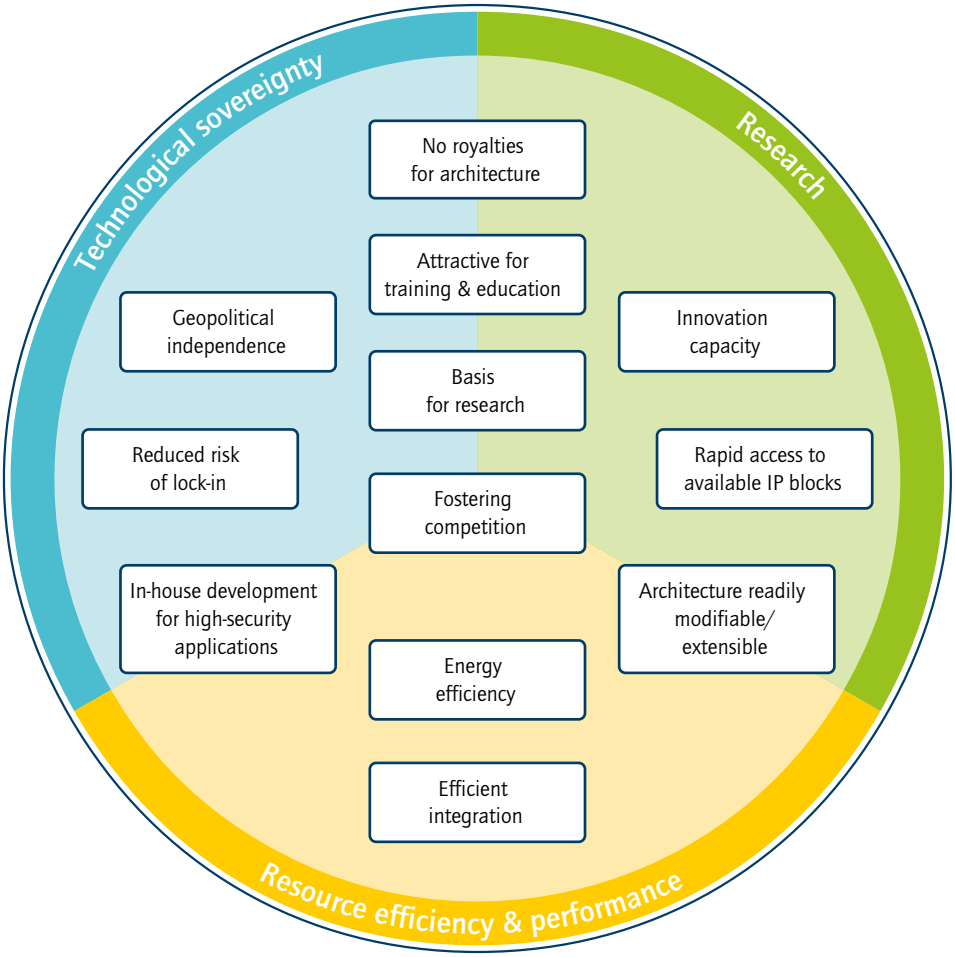

Figure 2: Clustering of anticipated opportunities with RISC-V into three categories (source: own presentation)

RISC-V and open source

RISC-V is often described as "open-source hardware" by the public, but this is misleading as RISC-V is not an implementation of a microprocessor, simply an open standard.

This term describes specifications or protocols which are in the public domain and free of restrictions. These standards provide a freely available basis for development and are intended to ensure interoperability between different systems and products. One good example of this is the TCP/IP internet protocol, which was developed as an open standard and is the basis for the functionality of the internet.

In contrast, open source denotes software which is freely available and can be created, modified and further developed by a community of developers. This software is subject to certain licence terms which disclose the source code and permit free use, customisation and redistribution. One well known example of open-source software is the Linux operating system.

While freely available open-source processor designs are an important element of the RISC-V ecosystem, there is absolutely no obligation to publish developments made on the basis of RISC-V. On the contrary, many commercial products based on RISC-V are already in existence which are protected as the IP of a company and were developed with entrepreneurial intent.

2.1 Opportunities with RISC-V for innovation and research

Using RISC-V as an open, collaborative basis for research offers the potential to drive innovation in chip architecture. Over the past two decades, high licensing costs and licensing-related hurdles have complicated research on processors and integrated system-on-chip (SoC)[15] designs. Moreover, copyright issues meant that results could not always be published in journals. RISC-V is giving rise to a new research environment which is injecting dynamism into both industry and academia. The active open-source community enables **rapid access to available processor IP**[16]**-blocks,** so providing a valuable starting point for activities with RISC-V and with innovative computer systems.

Technically, RISC-V is associated with fewer restrictions than licence-based architectures. The **architecture is readily modifiable and extensible** as well as scalable. Extension options are part of the standard. This enables researchers to develop new functions and extensions and integrate them flexibly into their chip designs without any need for coordination with a proprietary standard.

In addition, RISC-V is also **attractive for training and teaching**. Using the open standard offers students the opportunity to familiarise themselves with an open, scalable architecture independently of proprietary licences; moreover, **no royalties are payable for the architecture**. This enables application-oriented training in microelectronics and creates a solid foundation for future research activities. Integrating RISC-V into the activities of educational institutions will, in the long term, make it possible to address skills shortages in the electronics industry. If RISC-V is also deployed in companies, graduates will already be familiar with the technology, so improving links between academia and industry.

2.2 Opportunities for technological sovereignty with RISC-V

Using RISC-V means a **reduced risk of lock-in** for countries in general and for companies in particular since it is not dependent on proprietary technologies or architectures which require licences. This enables greater flexibility and freedom in the development of processors and integrated systems and their customisation to the individual requirements and constraints of the specific area of application. In international conflicts involving technology and trade embargoes, using an open standard protects the user's **geopolitical independence**.

Furthermore, a growing RISC-V ecosystem means companies can access existing implementations and customise them to their own requirements. Costs and/or royalties will then be incurred for the implementation or customisations, but not for the instruction set architecture. Two kinds of licence are conventional for proprietary instruction sets: firstly a regular licence which permits use of the instruction set in the licensee's products and secondly an architecture licence which is required for the licensee's modifications and extensions to the instruction set. Using an open instruction set in particular enables independent technology development for small and medium-sized enterprises (SMEs). This may in turn **foster competition**.

Simpler use in an academic environment and in teaching and training strengthens technological sovereignty since it increases **capacity for innovation** (e. g. skills in hardware design/development are fostered).

RISC-V can furthermore be used as a basis for **custom developments for high-security applications**, for example for communication technologies or in a military context. Especially in areas such as high-security applications or domain-specific platforms, an open standard allows greater adaptation to the use case and offers greater opportunities for custom security implementations. The reduced risk of lock-in and hoped-for improved and broader availability of IP blocks are further arguments in favour of using RISC-V in this context.

2.3 Opportunities for resource efficiency and performance with RISC-V

Depending on the use case, RISC-V can also improve processor resource efficiency and performance. As a result of the slowdown in Moore's law (see information box in section 1), there is huge potential for customised processors but this potential is more difficult to exploit with proprietary instruction sets due to restrictive licence terms. For example, the instruction set can be specialised for a specific use case and the **energy efficiency** of

15 | A system-on-chip integrates a number of functions of a programmable electronic system on a single chip and is thus typically smaller and more efficient than a traditional system with discrete elements.

16 | IP denotes intellectual property and, in this context, refers to tested processor designs.

the processor accordingly optimised. In hardware terms, RISC-V can permit tighter and **more efficient integration** of the microelectronic structures, enabling smaller chips and thus more chips per processed wafer.

2.4 Challenges when using RISC-V

It only makes sense to use RISC-V processors if the anticipated benefits outweigh the costs, effort and risks involved in switching to RISC-V, such as the necessary hardware implementation including verification and the development or purchase of a suitable software environment.

The challenges around RISC-V frequently reside in overestimating the potential of an open licence model since the costs of in-house development or integrating supplier IP or even open-source software may be underestimated. Likewise, a new open standard does not offer direct patent protection to the extent that semiconductor manufacturers are used to. These challenges are described in greater detail in section 4 of this publication.

The development costs for RISC-V-based processors vary greatly depending on use case and complexity. Smaller processors in particular can be developed with manageable effort. Freely available IP blocks and reference models whose functionality has already been demonstrated can be used as a starting point for development. Nevertheless, rigorous and systematic verification is required. Promising open-source and commercial tools – enabled by the open instruction set – are available to simplify this task.

The requirements profile for the software ecosystem depends on several factors, including the necessary software usability and the required degree of automation and robustness, but also on the number of functionalities required and the number of future software and system developers. If only a few people are involved in programming the RISC-V-processor and integrating it into a system, this team can work effectively with existing compilers and libraries and solve problems quickly and efficiently. In contrast, a system user's large development departments or even millions of users from the maker scene require a much higher level of quality, documentation, usability, well presented information (e. g. in the form of white papers or (video) tutorials), libraries, etc., which entails a very high level of effort for the ecosystem to be provided.

When it comes to general compilers, very good open-source solutions are already available,[17] which can be used with little effort. For instance, extensions with special assembler instructions (intrinsics) can be developed with manageable effort. With regard to special applications (e. g. HPC), where high-performance compiler efficiency offers a significant advantage, there is still a great need for development, with the situation being similar for the development of libraries. In the case of general, largely processor-independent libraries, which are usually implemented in high-level languages, little effort is involved since it is often possible to make use of existing code or general libraries. If special RISC-V processor features are to be utilised, the effort involved is correspondingly higher.

From a legal standpoint, the fact that the ecosystem is still under development and providers are only slowly becoming established leads to increased uncertainty among users of RISC-V solutions. As with any hardware IP, relationships with suppliers and service providers naturally have to be established, particularly with regard to guarantees for long-term support and liability issues. Structures to meet these needs, supported by European and national funding, still need to develop over the coming years.

17 | See for example https://gcc.gnu.org/ and https://clang.llvm.org/

3 RISC-V for architecture, system solution and application

This section describes the specific areas in which RISC-V can be used. Firstly, the use of RISC-V for different classes of processors and microcontrollers is considered from a technological perspective (see section 3.1). Various sectors that can benefit from RISC-V are then examined from an application-related perspective (see section 3.2).

3.1 Architecture and system solution

3.1.1 Deeply embedded and housekeeping

Current situation and statement of problem

Deeply embedded processors are microcontrollers of varying complexity which are usually deeply integrated and not directly visible to users. They often carry out specific highly specialised tasks in devices or systems.

Housekeeping processors are generally small processors which control the hardware units on the chip and perform less computationally intensive operations such as test support, rough data analysis in power-saving mode, action planning and the like. Housekeeping processors are usually, but not necessarily, programmed by the chip manufacturer itself.

Opportunities with RISC-V

The effort involved and necessary ecosystem for developing and supporting deeply embedded and housekeeping processors in RISC-V are comparatively small. It should, however, be considered that special applications such as safety or security (see section 3.1.5) will drive additional software requirements which can lead to not inconsiderable costs for the ecosystems. By switching to RISC-V-based solutions, companies can liberate themselves from the constraints of proprietary licences (see section 2.2).

Practical implementation

Since these solutions are visible only to the developers themselves, it is not obvious how widespread RISC-V is in this area. It can, however, be assumed that many companies are already using RISC-V-based solutions here.

3.1.2 Application processors

Current situation and statement of problem

Application processors are used as powerful central processing units (CPUs) in a wide range of applications. They may be programmed by a number of users and typically have standardised programming interfaces (e.g. Linux-based). They are used in devices such as laptops and smartphones, but also in industrial and automotive applications. These markets are currently dominated by solutions using proprietary instruction sets. On the other hand, RISC-V is becoming very important for application processors on the Chinese market, in particular for reasons of technological sovereignty.

Opportunities with RISC-V

Application processors typically have no particular specialisation, as they are intended to run generic applications; the expandability of RISC-V is thus of no advantage here.

However, the implementation of RISC-V architecture for application processors may be less complex and potentially more energy and space efficient, since (as yet) there is no need to ensure backward compatibility with older RISC versions. Heterogeneous multicore architectures[18] in particular can be implemented more easily. In addition, important extensions for application processors such as the RISC-V vector extension are considered to be particularly elegantly implemented in technical terms. The RISC-V concept for separating different access rights levels (privilege levels) can be considered leaner and more efficient than older architectures. Thanks to its particularly modular structure, RISC-V offers advantages for formal verification and thus for certifiable failure and information security.

Special challenges

Since application processors require very large amounts of software, it is not possible to rewrite the software. The key to efficient porting is therefore RISC-V support for major operating systems as an abstraction layer. For instance, Google has declared RISC-V the tier 1 platform for Android and the porting of Android to RISC-V is progressing swiftly. All the same, it is to be expected that it will be years before the quality which is characteristic of proprietary instruction sets is achieved. RISC-V is furthermore an officially supported platform of the Debian and Ubuntu distributions of Linux.[19] However, good hardware platforms are essential for developing such an ecosystem and it is here in particular that Chinese companies have got one step ahead.

Practical implementation

RISC-V-based application processors are primarily being developed in Asia. Important examples are Shanghai Saifang Technology Co., Ltd. (StarFive), which is distributing its application processor on a single-board computer (SBC),[20] and T-Head, a Chinese semiconductor manufacturer (part of Alibaba) which has also licensed its own RISC-V IP. The Chinese company Allwinner has developed an implementation which is also distributed as an SBC, while Taiwanese IP developer Andes is cooperating with the Japanese automotive supplier Renesas in the development of Linux-compatible automotive processors.[21]

18 | This describes architectures in which a combination of powerful and energy-efficient processors is used.
19 | https://riscv.org/news/2023/07/debian-gnu-linux-is-now-officially-supported-on-the-risc-v-architecture/
20 | https://www.starfivetech.com/en/site/boards
21 | https://www.renesas.com/us/en/about/press-room/renesas-selects-andes-risc-v-32-bit-cpu-cores-its-first-risc-v-implementation-assps

3.1.3 Special-purpose processors

Current situation and statement of problem

Special-purpose processors are designed for a specific class of applications and are optimised for these requirements. In the best case, for a given area, performance and efficiency advantages of a factor of 10 to 100 can be achieved over application processors. However, fundamentally new processor architectures or fundamental modifications to standard architectures are required to make this possible.

Opportunities with RISC-V

As an open instruction set architecture, a RISC-V-based solution can be flexibly adapted to the particular special application in question. For this purpose, a group of instructions and configuration options have been left free in the RISC-V instruction set to enable the definition of application-specific instructions. These instructions supplement the standard instruction set, i. e. software that can run on a standard instruction set will also be executable on a special-purpose processor. Accordingly, existing commercial and open-source software tools and libraries can continue to be used for software development. Further development of the architecture is enabling efficient processors which, even in comparatively large structure widths in the double-digit nanometre range which are inexpensive to fabricate, are competitive, thanks to their technical advantages, with non-optimised standard processors fabricated using the latest fabrication technologies (with a structure width of less than 5 nanometres).

Special challenges

Existing tools, in particular the support of special instructions as assembler instructions which can be inserted directly into the program code, are sufficiently available. One particular challenge, however, is the necessary in-depth understanding of the application domain, machine-oriented programming and hardware architectures. At present, there are insufficient appropriately trained specialists to achieve this.

Practical implementation

In recent years, a number of RISC-V special-purpose processors have been implemented in research institutes, at universities and in industry and their performance has been demonstrated.[22] However, it can be assumed that industry will not typically openly communicate activities in this field since special-purpose processors often provide the "unique selling points" for products.

22 | See Amor et al. 2021; Bringmann et al. 2021.

3.1.4 Embedded control

Current situation and statement of problem

Decisive criteria for applications in sensor and control systems with embedded electronics (embedded control) are often a low unit price and high reliability. Mobile applications additionally require high energy efficiency.

Opportunities with RISC-V

The ability to develop application-specific solutions with RISC-V without an architecture licence, for example for innovative sensor technology, can also make such solutions attractive for relatively small quantities of below 100,000 units per year. This can allow companies to create differentiating product features or start-ups to develop new, technically innovative applications.

In this scenario, RISC-V enjoys the advantage over other free architectures of a broader user base and a more modern technical approach. The extensive compatibility of RISC-V-based processors and field-programmable gate array (FPGA) solutions[23] increases security of supply while simultaneously reducing the cost of modifications to existing systems.

Special challenges

For many measurement and control applications, there are established standard products based on proprietary instruction sets which benefit from extensive software support and widespread experience in the embedded control community. Developing the know-how for integrating RISC-V-processors in applications is therefore a huge obstacle to the replacement of existing architectures. End-customers also often associate the use of domain-specific processors in products with lower reliability (e.g. in the field of power electronics) due to the smaller number of units and less widespread use. Rigorous quality control of the freely available IP is therefore important for industrial use. Legally, care must also be taken to ensure that the free IP does not infringe any third-party rights. In addition, developing new microchips remains a costly and risky enterprise, especially when it comes to integrating analogue functions for sensors and communication interfaces. Access to openly available RISC-V tools with assured quality can help overcome this obstacle.

Practical implementation

Widespread adoption of RISC-V has spawned numerous domain-specific microcontroller and system-on-chip (SoC) developers, both in the form of relatively small design houses and start-ups as well as major semiconductor manufacturers. For instance, Renesas launched a RISC-V-based embedded control processor for engine control systems in the autumn of 2022.[24] These activities provide special solutions for emerging sensor and control applications such as failure and quality prediction (e.g. Predictive-X), power electronics, personalised medical technology and use in drones and robots. Such solutions have energy efficiency, performance and unit cost advantages over standard products. The integration of AI capabilities in terminals in the form of embedded AI is becoming increasingly important in this segment.

23 | FPGA – a field-programmable gate array is an integrated circuit which can represent different logical circuits by means of software and so emulate different processors.

24 | https://www.renesas.com/us/en/about/press-room/renesas-extends-leading-risc-v-embedded-processing-portfolio-new-motor-control-assp-solution

3.1.5 Security

Current situation and statement of problem

For microprocessors used in secure applications, counterfeit products pose a high risk, being functionally identical but not offering the same security features as the original. There is often a dependency on uninspectable supply chains in which security of manufacture, for example in the chip foundry or during packaging and testing is not guaranteed.

"Trust anchors" (secure elements) are used to guarantee the security and trustworthiness of products and systems. These can be implemented either as a separate chip, such as the trusted platform module (TPM), or as an integrated component of a system-on-chip (SoC). TPMs play an important role in securing the boot process of laptops and desktop PCs, for example against attacks on the unified extensible firmware interface (UEFI) or bios start-up processes. Secure elements are also used to authenticate bank cards and IDs or hardware components, such as batteries and printer cartridges. Integrated in systems-on-chip, these are to be found in mobile devices or in automotive applications (e. g. HSM standardised among others by Bosch, BMW and Infineon in the EVITA project [25]).

Secure elements tend to be low in complexity but have very stringent requirements in terms of the trustworthiness of the electronics. If the trust anchor is compromised, any functions which refer to it are also no longer trustworthy. They therefore have to be specially implemented with secure hardware which is hardened for example against side-channel and fault attacks. There are also fundamental risks in terms of concealed hardware Trojans and possible backdoors if the chips are fabricated externally.

Opportunities with RISC-V

The open architecture of RISC-V allows companies to develop their own secure element hardware solutions using the existing ecosystem. The transparency provided by the available open source code for the hardware means that the design can be fully verified. Using open source code allows developers to create their own designs at reasonable cost and to easily integrate new functions, such as new cryptography algorithms.

Special challenges

Special measures have to be taken in the open RISC-V ecosystem to ensure source code quality and avoid Trojans. RISC-V security has to be achieved with complete transparency of the design, so ruling out "security by obscurity".

In order to further improve the use of RISC-V in this area, high-quality open-source designs must be available for which hardware implementations have also been evaluated in terms of security and continuously improved in the long term. While digital components can easily be shared as open source, security chips also require analogue circuits. At present, however, there are no suitable open-source alternatives for these components, as the results from the design tools of companies such as Cadence, Synopsys and Siemens EDA cannot be published. In addition, the technology parameters from fabrication which are required for analogue circuits are often not freely available. Moreover, security-critical processors also require a specific procedure for implementation on silicon and here too there are only proprietary solutions.

Practical implementation

There are already various open-source approaches to implementing secure elements with RISC-V, including OpenTitan from Google [26] and Caliptra specified by Google, AMD and Microsoft [27] Furthermore, Hensoldt Cyber has ongoing projects researching and advancing self-developed RISC-V chips for security.[28] Secure elements which can be integrated into systems-on-chips are, for example, available from the French company Tiempo Secure and the US company Rambus.

25 | See Henninger 2009.
26 | https://opentitan.org/
27 | https://www.chipsalliance.org/news/chips-alliance-welcomes-the-caliptra-open-source-root-of-trust-project/
28 | https://hensoldt-cyber.com/mig-v/

3.1.6 Summary

As the above explanations have shown, RISC-V is already in use in many types of processors for various reasons. The graph (see figure 3) ranks processor types by necessary development effort and value creation potential achievable with these products.

The development effort required for **deeply embedded and housekeeping** processors is low since their relatively low complexity allows them to be handled by just a few people within a company and means a large ecosystem (e.g. for software) does not have to be set up. Comparatively little effort is thus also involved in switching from existing solutions to RISC-V. However, since the processors of this class only perform generic tasks that can be carried out by many other readily available solutions, there is relatively little value creation potential. The main advantages of using RISC-V with these types of processor are the savings on royalties and independence from proprietary solutions.

A similar situation applies to **embedded control** processors. These are, however, specifically adapted to certain devices (e.g. sensors) and therefore require a greater degree of specialisation. On the one hand, this increases technical complexity and therefore costs. On the other hand, this specialisation and integration into a system can also be assumed to have higher value creation potential for in-house developments based on RISC-V, since they can be flexibly adapted to the particular target system.

Current estimates suggest that **special-purpose processors** using the RISC-V instruction set have the greatest value creation potential because this is where the technical advantages of the flexibly adaptable RISC-V architecture are most apparent. Since processors adapted for specific applications (e.g. AI accelerators or image processing) can boost performance by a factor of 10 to 100, the anticipated advantages far outweigh the development costs. This explains why increasing numbers of companies are investigating RISC-V.

Although the technical complexity of solutions in the area of **security** is on the low side, huge development effort is required here due to the stringent requirements in terms of trustworthiness; this is only justified if aspects such as technological sovereignty, for example for high-security applications, have to be taken into account. In particular if the hardware source code is openly available, the design can only be fully verified or validated in the physical presence of the chip, so increasing trustworthiness.

In most cases, RISC-V cannot yet be used profitably for **application processors** as these can only survive on the market where there is a very strong ecosystem. While the providers of proprietary licences have the necessary resources to ensure such an ecosystem, this is not yet the case for an open instruction set such as RISC-V. Here too, the use of RISC-V only makes sense if other (e.g. geopolitical) aspects come into play.

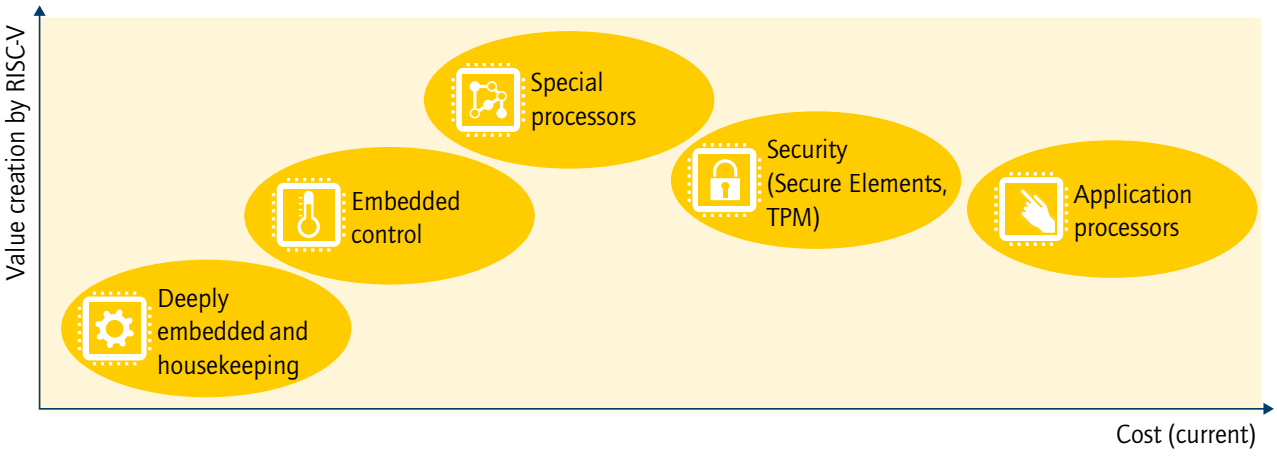

Figure 3: Clustering of the various RISC-V-based architecture and system solutions (source: own presentation)

3.2 Applications

This section describes some application scenarios which demonstrate a potential or already implemented use of RISC-V in an area relevant to Germany and Europe.

3.2.1 Education and research

Current situation and statement of problem

Over the past two decades, high licensing costs and licensing-related hurdles have complicated research on processors and integrated system-on-chip (SoC) designs when it comes to publication of the research results in scientific journals. One indicator of this is the decline in publications resulting from collaborations between universities and companies.[29] Using RISC-V opens up the possibility of reversing this trend and provides an opportunity to equip graduates with technical and industrially relevant know-how.

Opportunities with RISC-V

By using an open standard, universities, research institutions and companies can develop their own processors and platforms without licensing cost and so also present them at conferences or publish them in specialist journals. As a result, processors and system-on-chip (SoC) platforms have once again become the focus of research, something which has become particularly relevant with the slowdown in Moore's law and the emphasis on "more than Moore", i. e. the approach of not only increasing the number of transistors on a chip, but also improving the architecture and integration of functions on a chip. Universities can now devote themselves to research work that provides impetus for industrial development. In addition to pure research, it is now also possible to actually implement the developed chip designs and create chip layouts, something which was often difficult and expensive in the past. Using RISC-V now enables universities and companies to fabricate and test their own chips.

A further advantage of RISC-V in academic research is the possibility of building a complete ecosystem without much effort. A wide range of supporting tools and software can be used when it comes to developing a RISC-V-based processor core. These include compilers, operating systems and other development environments which have been specially designed for RISC-V.

Prior to the introduction of RISC-V, researchers generally developed individual solutions and architectures, which resulted in fragmentation. With RISC-V as a common basis, universities can build on a uniform foundation and benefit from the advantages of a common architecture. This also enables better reproducibility and comparability of research results, something which has often not been the case in the past.

Special challenges

Since the circumstances in a university environment differ from those in industry, components of the RISC-V ecosystem developed in an academic context usually do not meet industry's requirements for usability and reliability. Cooperation projects between science and industry are a useful way of making academic work usable in industry.

Practical implementation

ETH Zurich and the University of Bologna have for many years been driving forces in RISC-V and have made significant contributions to creating standards which today serve as a foundation and facilitate use of and cooperation in the field of RISC-V research and development. The work of these universities provides the basis for current funding projects and is helping to foster the adoption and development of RISC-V.

RISC-V is used, to varying degrees, in almost all universities, for example at Hochschule München University of Applied Sciences (HM) where application-oriented use of RISC-V is studied from the very first semester in bachelor's degree programmes. The curriculum is designed to ensure that students come into contact with the instruction set from the outset, so enabling continuous consolidation and application of RISC-V during their course of study. Students will subsequently also be able to apply their knowledge in research and industry. Cooperation between academia and industry is now being promoted in the context of specific projects[30].

29 | https://www.stiftung-nv.de/de/publication/who-developing-chips-future-reloaded
30 | https://elektronikforschung.de/projekte/tristan

3.2.2 Telecommunications

Current situation and statement of problem

The telecommunications industry has undergone a transformation over the past two decades from a very much hardware-centric industry with customer-specific hardware implementations towards more software-based solutions. As a result this has advantageously led to less frequent changes in hardware development, faster project innovation, greater availability of personnel and more flexible products. The transition from hardware- to software-centric solutions is, however, not yet complete, in particular for commercially usable products.

Moreover, telecommunication products themselves are increasingly moving towards edge computing, i. e. edge devices (consumer product, WiFi/5G access point or an aggregation node further up the chain) are becoming programmable and capable of computation so that services can run on the edge rather than in the cloud. There are two reasons for this: firstly, transferring data to the cloud for centralised processing has an environmental impact and is costly. Secondly, data protection is playing a part in driving edge processing because it ensures that sensitive consumer data do not leave the building and are thus protected from unwanted access.

In a nutshell – the telecommunications world is becoming a software-centric world. The two major proprietary instruction set architectures currently predominate here. Other instruction sets (Power Architecture from NXP/Freescale/Motorola and various digital signal processors (DSPs)) are still used, but only on a company-specific basis. This is potentially a threat to technological sovereignty.[31]

Opportunities with RISC-V

RISC-V can act as a counterweight to proprietary providers and restore competition between multiple suppliers. In addition to the general advantages mentioned above such as extensibility, RISC-V also has the advantage of being an open standard, making it more resistant to geopolitical developments. A reliable instruction set architecture is particularly important in a software-heavy field. In the medium to long term, this could lead to more competition, which in turn means higher quality and faster innovation for everyone involved. There is also a cost advantage in that lower development and unit costs allow RISC-V-based products to compete effectively in the market.

Special challenges

As described above, telecommunication devices, if they are software-based at all, are based on the two major proprietary instruction set architectures. Over the past two decades, millions of lines of code have been written for these architectures. Since telecommunication products are increasingly subject to CISA/ENISA[32] and other cybersecurity considerations, the barrier to change (software migration costs) in this code base is getting higher, especially as the performance benefits of moving to RISC-V have not (yet) been embraced by the industry.

Practical implementation

Since RISC-V is a new technology, no fully RISC-V-based telecommunication devices are as yet known on the market. It may, however, be assumed that subsystems of telecommunication devices will be converted to RISC-V or that compatibility with systems currently in use will be ensured.[33] The development cycle for chips and products in telecommunications is around three to five years. This means that investments in the choice of future instruction set architectures will have to be made now, the industry being open to RISC-V-based solutions.

31 | See acatech 2021.

32 | The Cybersecurity and Infrastructure Security Agency (CISA) and the European Union Agency for Cybersecurity (ENISA) are respectively the US and European cybersecurity agencies.

33 | https://github.com/google/android-riscv64

3.2.3 Computing and data centres

Current situation and statement of problem

Increasing digitalisation and connectedness are continuously driving global demand for computing capacity. This demand has recently also been driven by new artificial intelligence applications such as image recognition for autonomous driving or in generative models for creating image and text output. At the same time, however, data centre operators and users are becoming increasingly aware of energy consumption and the need for efficient use of resources in this highly competitive environment.

In parallel, the slowdown in Moore's law (see information box in section 1) is bringing new challenges. Since the miniaturisation of microelectronic components is reaching its limits, there is a need to identify new solutions such as multicore approaches and special-purpose processors. At present, processors with proprietary instruction sets which use corresponding accelerators still dominate, but the field for new architectural approaches is opening up.

Opportunities with RISC-V

RISC-V is a flexible architecture which enables custom processors for data centres using specialised hardware. More efficient platforms can be created by using on-chip or on-package solutions such as chiplets[34] RISC-V also has potential for the development of a broad ecosystem around such an architecture. RISC-V's flexibility and capacity for innovation could help to increase diversity and competitiveness in this area and open up new opportunities for customised, high-performance data centres.

Special challenges

In addition to the already high demands on the competitiveness of powerful processors with minimal structure widths (3 to 5 nanometres), there is also a need for an efficient computer architecture with extensions independent of the instruction set as well as an efficient software ecosystem. While optimised solutions are already available for proprietary instruction sets in many areas, this is not yet universally the case for RISC-V. Comprehensive optimisation of the RISC-V software ecosystem is vitally important if it is to be possible to make full use of this architecture's advantages.

Practical implementation

While Europe does not to date have any commercially available RISC-V-based processors for computing and data centres, there are very successful companies in this field in the USA (SiFive[35]) and in China (Starfive[36]) In Europe, RISC-V is being used in the context of the European Processor Initiative (EPI) at the Jülich Supercomputing Centre (JSC).[37]

34 | Chiplets are prefabricated modular chip components that can be combined to form a complete integrated system for specific applications.
35 | https://www.sifive.com/cores/performance
36 | https://www.starfivetech.com/en/site/activity_details/965
37 | https://www.fz-juelich.de/en/ias/jsc/research/funded-projects/highlight-projects/european-processor-initiative-epi

3.2.4 Automotive and mobility

Current situation and statement of problem

The automotive industry is currently facing the challenge that its products have increasingly to be seen as "computing and data centres on wheels". Against this background, vehicles are being redesigned from the ground up, no longer being numerous independent systems with simple control units but instead systems consisting of a few interconnected computers. This approach is also known as "zonal architecture".

At the same time, many classes of vehicle are moving away from fossil fuels towards electrical power sources requiring numerous additional electronic components, for example for battery management and charging electronics.[38]

Furthermore, the heterogeneous field of several instruction sets can be observed to be moving towards a monopoly situation: while instruction set architectures were highly heterogeneous into the 2010s, the field is increasingly consolidating due to better cost efficiency and flexibility with regard to suppliers for OEMs. This situation is a potential threat to technological sovereignty, in particular for exports to and manufacturing in China.

Opportunities with RISC-V

RISC-V can act as a counterweight to proprietary providers and promote competition between multiple suppliers. As described for the previous fields of application, it is above all the extensibility of the instruction set which gives RISC-V huge innovation potential for new, efficient solutions. In addition, independence from proprietary licences offers advantages in terms of technological sovereignty, for example enabling global exports without trade restrictions.

Special challenges

Long development cycles of up to ten years and strong cost competition between manufacturers must be taken into account in the automotive industry. In this environment, it is economically challenging for suppliers of semiconductor components to develop and reliably offer a number of product variants, the automobile manufacturers making the decision as customers as to which products can be offered for sale. At present, established suppliers are preferred due to the extensive ecosystem and the better price/performance ratio of the processors. This leads to a chicken-and-egg situation – the supply of RISC-V-based products will only be sufficient when demand is strong enough. However, demand will not develop if no satisfactory offer is available to meet current demand.

The "computing and data centre on wheels" concept demands ever more variant solutions known from high-performance computing (HPC). The differentiation between HPC and non-HPC in research and development is making it difficult to exploit synergies. In addition, this application requires processors which can better be described as tensor processing units (TPUs) for AI applications or as graphics processing units (GPUs) for graphics. Although RISC-V does offer vector instructions, it does not have a specific TPU or GPU instruction set profile.

Practical implementation

Since the technology is still too new, there is currently no entirely RISC-V-based vehicle. While the use of individual embedded RISC-V cores is to be anticipated in the coming years, customer-programmed processors in the automotive industry will continue to be based on proprietary solutions running the respective brand's software. It is expected that the next generation of vehicles will be based entirely on these solutions until 2029 and that the leap to RISC-V may not take place until 2033. The development of chips for the automotive sector requires a considerable lead time compared to the actual manufacturing of the vehicle. At the same time, there is some concern about a single provider's strong monopoly position. The industry is therefore keeping a close eye on developments and is seeking out solutions for reducing dependence on a single architecture and improving interchangeability and compatibility. It is for these reasons that the semiconductor manufacturers Robert Bosch GmbH, Infineon Technologies AG, Nordic Semiconductor, NXP® Semiconductors and Qualcomm Technologies, Inc. have joined forces to invest in a company which is intended to foster the global adoption of RISC-V through the development of next-generation hardware.[39]

38 | https://www.usitc.gov/publications/332/executive_briefings/ebot_amanda_lawrence_john_verwey_the_automotive_semiconductor_market_pdf.pdf
39 | https://www.bosch-presse.de/pressportal/de/en/leading-semiconductor-industry-players-join-forces-to-accelerate-risc-v-257024.html

3.2.5 Aerospace and defence

Current situation and statement of problem

In both commercial and military aviation, the avionics components responsible for aircraft control are subject to the most stringent requirements in terms of reliability and certifiability. Two redundant, but technically different systems are often specified for a single task in order to minimise the risk of total failure during flight. Still more so than the automotive industry, aircraft manufacturers are dependent on suppliers who can ensure product availability and support for decades since changing a system results in very costly recertification for approval, training and insurance. In commercial aviation, support should ideally be possible worldwide.

In recent years, established suppliers have gradually discontinued products based on PowerPC and SPARC processor architectures that are currently in service but are technically outdated, so there is a need to switch over to new architectures. It is currently unclear whether aircraft manufacturers will develop the next generation of avionics components themselves or whether suppliers will be able to develop and offer follow-on products with sufficient security of supply.

The situation is somewhat less acute for unmanned space flight since such missions are automated, which means that malfunctions do not pose a direct risk to humans. Nevertheless, comparably long development times with huge capital costs prevail, resulting in stringent requirements with regard to reliability and certifiability of the components used, not least on the part of insurers.

Opportunities with RISC-V

The existing RISC-V ecosystem would be a good starting point for new developments in aerospace components. Due to the industry's stringent safety and certifiability requirements, standard components are often inadequate. Given strengthened design skills and the free availability of RISC-V, chips for aerospace components could be developed in-house. Flexible extensibility means that the stringent requirements with regard to safety and special requirements for space applications (e.g. radiation resistance) could be met. Using RISC-V would eliminate the constraints of a proprietary instruction set and could strengthen the technological sovereignty of the participating companies.

Special challenges

Setting up an ecosystem for a RISC-V-based development would be complex in technological and personnel terms, in particular due to this industry's stringent requirements. Certified tools are required for software development, and redundant systems often require two completely different implementations of the same function. It remains to be clarified whether both implementations can be based on RISC-V and aircraft manufacturers in particular are put off by this effort because the supplier structure which has so far been used is easier to manage. Suppliers of new products must offer the customary level of reliability, something which it is difficult for start-ups to guarantee.

Practical implementation

The use of RISC-V for aerospace is being investigated in various European cooperation projects with participants from industry and academia, such as De-RISC[40] and Selene[41]. Wider adoption of RISC-V in this industry is dependent on the development of the ecosystem as a whole.

40 | https://derisc-project.eu/
41 | https://www.selene-project.eu/

3.2.6 Industrial processors and Industry 4.0

Current situation and statement of problem

Automated industrial manufacturing makes use of microelectronic components of all levels of complexity ranging from simple microcontrollers to complex application processors and special-purpose processors. Due to the great potential for losses caused by production downtime or faulty production, these components have to meet the most stringent requirements in terms of reliability as well as functional and IT safety/security, especially in an increasingly interconnected and real-time-oriented environment. While in some use cases it is sufficient to use products with commercially available standard components for microcontroller and application processors, such safety-critical applications have a great need for differentiated electronics based on in-house developments with application-specific extensions. Stable supply chains are necessary for all these components. In addition, using components containing proprietary licensed functional elements means that trade restrictions also apply to the products in which these components are used.

Opportunities with RISC-V

While RISC-V does not offer any noticeable advantages over proprietary instruction sets in terms of performance from an application perspective, there is a clear benefit for the industry from an organisational and economic point of view since dispensing with proprietary instruction sets means that companies are not dependent on the restrictions associated with the use of such instruction sets. Companies can independently develop and integrate application-specific extensions. This aspect is particularly of interest in relation to components of low complexity (e. g. for a real-time capable deeply embedded application), as the effort involved for the companies and the required expertise are manageable meaning the economic advantages can be obtained. In addition, as an open and licence-free architecture, RISC-V is not subject to the trading restrictions of proprietary licences. Of the three possible levers for enforcing trade restrictions – blocking design IP, chip development tools and fabrication process – the availability of design IP would appear already to be being successfully addressed.

Furthermore, the number of freely available open-source implementations of design IPs for RISC-V is growing and these are a valuable starting point for chip developments based on them.

Special challenges

A central challenge is to build and maintain a stable and efficient ecosystem for RISC-V. This includes the availability of expertise, design IPs, specialised design and verification tools and the necessary documentation for certification in accordance with relevant standards for functional and IT safety/security. Medium-sized companies in particular may not find the supporting software development tools (e. g. tracers) that they are used to from products with proprietary instruction sets. Although relatively small teams can familiarise themselves with the technology, they often need support to ensure that their products comply with the relevant standards. For large development departments, a robust ecosystem is crucially important in order to be able to develop the usually large number of product variants efficiently and reliably. Unlike with pure software products, it is difficult subsequently to rectify a fault in microelectronic components which have already been delivered, the hardware components instead having to be replaced at great expense.

Practical implementation

In order to strengthen the ecosystem for RISC-V and facilitate its use in industrial processors, it is crucial to make the necessary tools available and maintain them on an easily accessible platform, something which is already being driven by initiatives such as the Virtual Design Platform as part of the European Chips Act [42] and the Bavarian Chip Design Centre [43] The platforms are intended to provide developers with access to design tools, training materials and support to facilitate the implementation of RISC-V in industrial processors. Such initiatives can further foster the acceptance and adoption of RISC-V in industry, so strengthening the flexibility and independence of companies while simultaneously meeting the requirements for reliability as well as functional and IT safety/security.

42 | https://digital-strategy.ec.europa.eu/en/factpages/chips-europe-initiative
43 | https://www.iis.fraunhofer.de/de/ff/sse/bayerisches-chip-design-center.html

3.2.7 Summary

Figure 4 plots the various discussed applications by value creation potential and development costs. **Education and research** stands out, offering as it does very high potential at low cost. This assessment is based on the fact that both university and industrial research can act much more flexibly and quickly by using a free instruction set, as no agreement with a licensor is required. Moreover, innovative modifications can be made to the instruction set. The advantages of an open community which makes tools and software freely available are particularly important in the early development phase, especially in university research. It should, however, be noted that the timeframes in a research context are significantly longer than in the other applications and the value creation here will therefore only be apparent much later.

In contrast, higher quality software tools are required for **industrial processors** in order to ensure the required stability and quality of the products. In addition, it is often necessary to move away from established structures, which results in high costs for companies. In particular in **telecommunications** and **mobility and automotive**, a high level of dependency on software is one major reason for the high costs that would be associated with a change of instruction set. In addition, **mobility and automotive** in particular has stringent safety and certification requirements. In this case, new providers must first establish themselves and be able to demonstrate the necessary standards before a switch is possible. Although the standards for certification in **aerospace and defence** are likewise very high, RISC-V-based solutions are already in use here. The key difference from the automotive sector is in quantity, which is significantly smaller for aerospace, and in some cases even an individual solution. The small unit volumes mean that the required development costs are lower than in industries with high unit volumes, but at the same time this also explains the lower value creation potential. However, the greatest value creation potential is in **computing and data centres**, this being explained by the technical advantages that RISC-V-based processors can offer for AI applications together with the current strong demand for computing power for these applications.

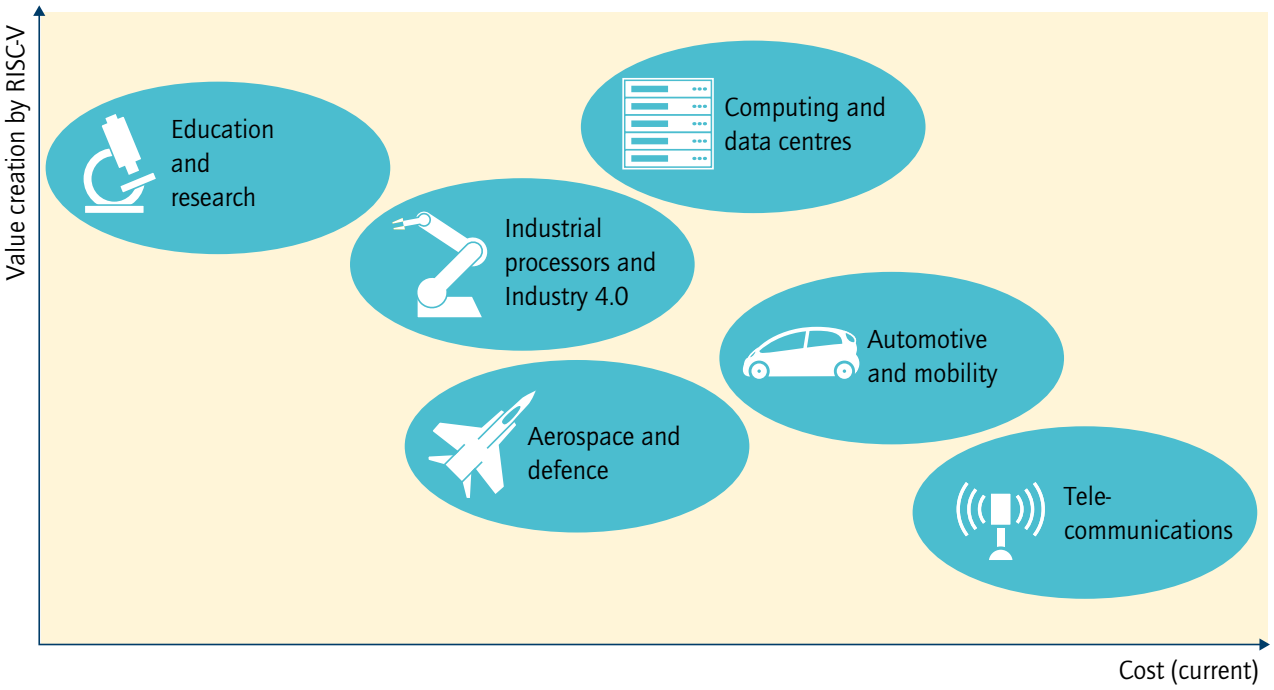

Figure 4: Clustering of applications (source: own presentation)

4 Findings and recommendations

The findings from section 3 (see figures 3 and 4) are used below as a basis for identifying measures for further strengthening RISC-V. These findings will firstly be broken down by the various types of processor as the actions required for each are very different. The specific recommendations will then be associated with the various stakeholder groups.

There is no specific action required to improve the situation for **deeply embedded and housekeeping processors** as the existing circumstances are already sufficient to enable companies to use RISC-V successfully and indeed it is often already in use here. There is a certain value creation potential for **embedded control processors** so it is to be expected that companies will increasingly consider using RISC-V-based processors for their devices. Strengthening the RISC-V ecosystem would thus accelerate innovation and enable value creation. This trend is continuing with advanced **special-purpose processors** where there is huge potential for innovation but proprietary licences make it difficult for start-ups and SMEs in particular to realise this potential. This area would benefit considerably from the use of RISC-V, but is dependent on a strong ecosystem. Technological sovereignty is the focus for **security processors**. RISC-V-based solutions are possible and should be considered if the effort involved is outweighed by the sovereignty gained. **Application processors** based on RISC-V are currently out of reach for Europe, placing as they do very stringent requirements on the quality of the ecosystem in terms of expertise, software tools and certifiability. At the same time, highly developed commercial products are already available for which the flexibility of RISC-V offers no technical advantage; nevertheless, a RISC-V-based application processor would make sense from the standpoint of technological sovereignty. However, this requires far-reaching institutional funding, as is being successfully implemented in Asia[44], and significant support for start-ups, as is the case in the USA.

In a nutshell, the priority should be on building and strengthening the RISC-V ecosystem in the long term. Activities which are already under way, such as the joint investment in a company recently announced by major semiconductor manufacturers,[45] should be further expanded and supported. This requires both a long-term vision and investment in key areas such as compiler development, training courses, specialist literature and the promotion of certified standards. The development of professional consulting and support services for RISC-V could facilitate its adaptation and integration. Companies should be more strongly encouraged to make an active contribution to RISC-V International and to vigorously pursue standardisation.

Recommendations to policy makers

- Investment in projects relating to RISC-V should be seen as a tool to strengthen expertise in microelectronics, in particular in design capabilities. In the context of agreed investments in fabrication capacity and in view of the prevailing skills shortages, such strengthening is an important contribution to increasing technological sovereignty.
- A functional ecosystem including software tools, hardware designs and skills is an essential factor in the success of RISC-V. Funding should therefore not focus solely on the development of individual chips but rather on supporting and sustainably developing all aspects of the RISC-V ecosystem in order to strengthen the electronics industry in the long term. For example, contributions to the content of RISC-V International arising from research projects could be rewarded.
- Existing funding structures with a lead time of several years may be too sluggish for short-term innovation. It should therefore be investigated whether faster innovation funding is possible in order to develop a dynamic start-up culture, as already exists in the software sector. For many start-ups, the usual self-financing portion of funding programmes is a stumbling block which should be reviewed as part of the desired strengthening of the start-up sector in the semiconductor industry.
- In order to strengthen training at universities, Germany and Europe should expand RISC-V funding programmes, particularly with regard to the growing demand for semiconductor specialists. These activities should also include lifelong learning approaches to enable a closer link between industrial training and academic education.

44 | See for example the activities in India (https://pib.gov.in/PressReleasePage.aspx?PRID=1820621) und China (https://github.com/OpenXiangShan/XiangShan)

45 | https://www.bosch-presse.de/pressportal/de/en/leading-semiconductor-industry-players-join-forces-to-accelerate-risc-v-257024.html

Recommendations to business

- Companies often harbour a belief that products using RISC-V cannot achieve the quality required for commercial products; however, it has been shown that an increasing number of commercial products containing RISC-V are coming onto the market. It is therefore recommended to review the use of RISC-V. Embedded control and special-purpose processors in particular are seen as having great value creation potential.
- Since open standards have been very successful in the past, German and European business should also actively help to shape RISC-V as an open standard in order to be able to include its own requirements in further development.
- Achieving the necessary quality means professionalising and strengthening the ecosystem, as has already been successfully established for open-source software.[46] While in the case of proprietary solutions, this is a task for the licensor, in the case of licence-free solutions it is the responsibility of the companies which use the standard to maintain the ecosystem through professional software tools, training and further development of the standard. Participation in cooperative further development is recommended in order to ensure the necessary quality of the ecosystem.
- A key advantage of RISC-V is its independence from proprietary licences, which ensures technological sovereignty. However, companies often do not take this aspect into account in quantitative terms when weighing up economic considerations. In the light of the experience of the early 2020s, it is recommended that the economic aspect of technological sovereignty should always be considered with regard to risk assessment and resilience.

Recommendations to academia

- As no licences are required for the use of RISC-V and no costs are incurred when using the standard, it is organisationally straightforward to use it in academic teaching. Suitable teaching provision can enable students to familiarise themselves with the subject matter and gain valuable practical experience.
- Because the instruction set can be freely modified, innovative research projects are possible without such modifications having to be agreed with the licensor.
- Due to the anticipated widespread adoption of RISC-V, graduates are likely to have a need for lifelong learning opportunities. It should be checked whether learning material from current degree programmes can be made publicly available for this purpose.

46 | See Linux Redhat; https://www.redhat.com

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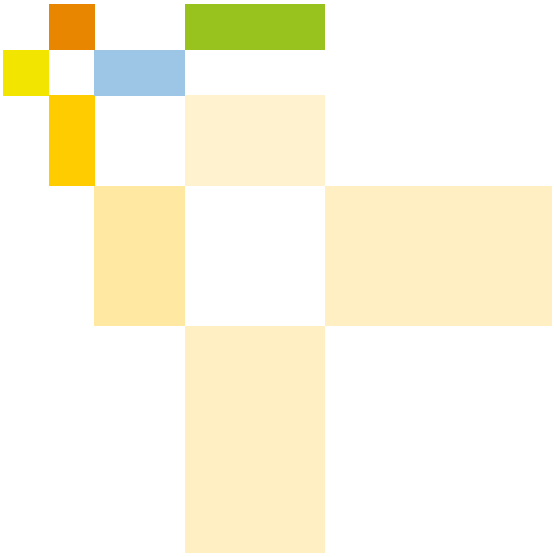

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Series editor:

acatech – National Academy of Science and Engineering, 2024

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Recommended citation:
Kutter, Chr. (Ed.): *RISC-V: An Open Standard for Chip Development* (acatech IMPULSE), Munich 2024.
DOI: https://doi.org/10.48669/aca_2024-5

Bibliographical information published by the Deutsche Nationalbibliothek.
The Deutsche Nationalbibliothek lists this publication in the Deutsche Nationalbibliografie;
detailed bibliographical data are available online at http://dnb.d-nb.de.

Coordination: Dr. Patrick Bollgrün, Dr. Paul Grünke
Translation: Paul Clarke and Charlotte Couchman, Lodestar Translation
Layout concept: Groothuis, Hamburg
Cover photo: © kynny/Shutterstock.com
Conversion and typesetting: Heilmeyer und Sernau Gestaltung

The original version of this publication is available at www.acatech.de

The chip crisis in early 2020 clearly revealed how dependent German and European industry was on the supply chains for microelectronic components. Despite experts repeatedly emphasising the importance of microelectronics to Europe's capacity for innovation, shortages occurred which threatened major industrial sectors. In response, the European Chips Act was passed and the establishment of chip fabrication facilities in Europe was accelerated.

In addition to fabrication, a key factor in ensuring Europe's technological sovereignty is to strengthen innovative chip development capabilities by providing appropriate specialist personnel. In this context, the RISC-V open standard instruction set architecture holds great promise because it eliminates many of the constraints of proprietary command sets.

Since RISC-V is characterised by a very variable architecture, numerous different use cases are conceivable. This acatech IMPULSE discusses the opportunities and threats of different scenarios and outlines options for decision-makers in business and politics.